SPECIFICATION AMENDMENTS

Please amend paragraphs 0007 and 0039 on pages 2 and 9, respectively, as follows:

[0007] Multiple state flash EEPROM structures using floating gates and their operation are described in United States patents nos. 5,043,940 and 5,172,338, and for structures using dielectric floating gates in aforementioned United States application serial no. 10/280,352, publication no. 2003/0109093 A1. Selected portions of a multi-state memory cell array may also be operated in two states (binary) for various reasons, in a manner described in United States patents nos. 5,930,167 and 6,456,528.

[0039] If desired, a plurality of arrays 400, each with its associated X decoders, Y decoders, program/verified circuitry, data registers, and the like are provided, for example as taught by U.S. Patent 5,890,192, issued March 30, 1999, and assigned to Sandisk Corporation, assignee of the present application, which patent is hereby incorporated herein in its entirety by this reference. Related memory system features are described in co-pending patent application serial no. 09/505,555, filed February 17, 2000 by Kevin Conley et al., now patent no. 6,426,893, which application is expressly incorporated herein in its entirety by this reference.

Please make a correction to paragraph 0076 on page 22, as follows:

[0076] The consolidation operation described with respect to Figures 12A-12C uses available erased pages in the E1 block because the number of pages being updated at one time is less than a ~~present~~ pre-set number, such as one-half the number of pages in the E1 block, one of the criteria that may be set for using the block E1. If more than those number of pages are being updated, the updated data are written directly into the E2 block, as previously described with respect to Figures 11A-11B. A different consolidation operation occurs when the number of pages of a logical block that are being updated at one time exceeds the predetermined number, and no other established criteria for using the block E1 exist, but where one or more updated pages of that logical block have previously been written into the E1 block. In this case, the

updated blocks are written directly into the E2 block. An operation of the memory system controller that handles this situation is described with respect to Figures 13A-13C.